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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/602,020	REBLEWSKI ET AL.	
	Examiner	Art Unit	
	AKASH SAXENA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,8-10 and 16-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8-10 and 16-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-2, 8-10 and 16-32 has/have been presented for examination based on amendment filed on 11/24/2008.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/29/2008 has been entered.
3. Claim(s) 1, 2, 8, 9, 19, 20, 29, 30, 31 and 32 is/are amended.
4. Claims 1, 2, 8, 9, 16-19 are rejected based on amendment under 35 USC 112 second paragraph.
5. Claim(s) 1-2, 8-10 and 16-32 remain rejected under 35 USC § 103.
6. This action is made NON-FINAL. The examiner's response is as follows.

Response to Arguments for Claim Rejections - 35 USC § 112¶2nd

7. Applicant's arguments are considered, however are found to be unpersuasive, and on the contrary buttressing examiner's position in the Advisory action that the "state data" and "data of interest are cyclically dependent on each other and none of them are clearly defined.

Response to Arguments for Claim Rejections - 35 USC § 103

(Argument 1) Applicant has argued in Remarks Pg.9:

> Swoboda merely discusses a compression map as shown in fig. 19 in order to process selected data (i.e., data of interest) (data byte 1, data byte 2, and data byte 5) from packet 91 as shown in fig. 9. (Paragraph 121 .) However, Swoboda fails to discuss any thing about the location of

> selected data being different when processing different packets. Moreover, Litt and Tausheck fail to remedy the deficiencies of Swoboda. Litt merely discusses a bandwidth manager for assisting in the offloading of internal state data (column 3, lines 28-42) while Tausheck merely discusses chained direct memory access operations (column 2, lines 20-46).

(Response 1) Swoboda shows a sample compression map with the ***rationale*** how the data of interest is selected from the state data. Specifically Swoboda [0121] teaches:

> [0121] In FIG. 19, the data header packet at 190 could correspond to the packet 91 in FIG. 9 above, with the data compression map transmitted thereafter as a continue packet 192. Thereafter, as shown in FIG. 19, the data byte transmission proceeds analogously to that shown in FIG. 9. Considering specifically the data compression map shown in FIG. 19, this map is basically a byte (8 bits) of data wherein a bit value of 1 indicates that the corresponding new data byte is the same as the corresponding previous data byte, and therefore will not be sent, and wherein a bit value of 0 indicates that the corresponding new data byte differs from the corresponding previous data byte, and therefore will be transmitted. In FIG. 19, the shaded bytes correspond to the 0s in the data compression map, and only these bytes will be sent. The trace packet decoder in FIG. 2 can easily decode the data compression map and determine therefrom which bytes are being transmitted and which bytes are merely duplicated and therefore not transmitted.

It is obvious that not every sample state data layout would look identical to the exemplary sequence presented in Fig.19. A different sequence of bytes, other than the one listed in Fig.19, would result in different bytes selected based on the underlined rationale above. Hence applicant's argument is unpersuasive. Claim 20 is rejected similarly.

(Argument 2) Applicant has argued in Remarks Pg.:

> However, Litt merely discusses bandwidth manager 125 that selects data from two or more data streams within an integrated circuit, where the incoming data sources represent state data from regions within the integrated circuit. The selection of the incoming data stream is determined by signal VP (as shown in fig. 2 but not numbered), which may be based on a configuration and status register. (Column 8, lines 34-48.) However, Litt is silent about selecting data from samples of state data in which the bit locations are different **[1]** , and thus does not teach the feature of"a first select logic device configured to receive samples of state data, to select data of interest from each of the samples of state data, the data of interest having non-contiguous bits, and to sort the data of interest such that the non-contiguous bits become contiguous; wherein selected bit locations of the data of interest from at least two samples are different."

(Response 2) As per [1], this teaching is obvious from the Fig.19 of Swoboda. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Regarding Claim 29 and 31

(Argument 3) Applicant has argued in Remarks Pg.11-12:

> However, as shown in fig. 22, Swoboda merely discusses pin manager 224, which routes a single stream of transmission packets to desired pins of a debug port. (Paragraph 128.) However, Swoboda is silent about routing a plurality of packet streams and thus fails to even suggest the feature of "determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates, wherein one of the plurality of pins is shared by at least two trace data chains."

(Response 3) Examiner disagrees with applicant as Swoboda is particularly concerned with resizing the trace packets of various widths to conform to the plurality of pins available for transmission. Applicant has cited [0128], which at the end discloses adjusting the width of the trace packets as:

> [0128] FIG. 22 illustrates pertinent portions of exemplary embodiments of the trace export portion of FIG. 2. As shown in FIG. 22, the trace export portion includes a FIFO buffer coupled to a transmission formatter 220. The FIFO buffer receives the composite trace stream produced by the stream combiner 85 (see also FIG. 8). **The transmission formatter 220 outputs a stream of transmission packets to a pin manager 224 which routes the packets to desired pins of, for example, a debug port on the target chip.** Continuing with the above-described 10-bit trace packet example, **the stream combiner 85 produces a composite stream of 10-bit trace packets. The trace export portion, including the FIFO buffer and transmission formatter 220, transforms the trace packets of the composite packet stream into a stream of transmission packets that can have a different bit width than the 10-bit trace packets.** This stream of transmission packets is sent sequentially from the pin boundary of the target chip to the **trace recorder** of FIG. 2. The transmission packets can be delivered to the trace recorder via, for example, the debug port or another system bus port.

Further, evidence that the plurality of trace pins are mapped to the trace stream is shown in Swoboda [0017], [0051], [0052], [0058], [0073], [0092], [0094] at least.

Further as presented the claim reads on the teaching presented in Swoboda. Please see the claim mapping in the rejection. Claim 31 is rejected likewise below.

Claim Rejections - 35 USC § 112¶2nd

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 1, 2, 8, 9, 16-19 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1, 2, 8, 9, 16-19 (Updated)

Above claims amend language qualifying the data as “state data” and subset of that as “data of interest”. However neither claim nor specification defines “state data” and how a subset of that is selected to arrive at “data of interest”. Further as detailed by applicant specification ¶28 and ¶38 define the "state data” and "data of interest" to be cyclically dependent on each other and are not defined clearly.

Regarding Claim 1 (new)

Amended claim now recite:

> “...selecting a second data of interest from the second sample of state data, wherein the second data of interest is a second subset of bits of the second sample of state data and wherein bit locations of the first data of interest and the second data of interest are different.”

How the first and second data of interest are different is not claimed. It is not clear if they their location is different from each other or different from the first and second data of interest of first sample of state data respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-2, 8-10 and 16-32 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2002/0065642 A1 by Gary L. Swoboda (Swoboda hereafter), in view of U.S. Patent No. 6,816,989 issued to Timothe Litt (Litt hereafter), further in view of US Patent No. 6092127 issued to Eric G. Tausheck (Tausheck hereafter).

Regarding Claim 1 (Updated 2/12/09)

Swoboda teaches a method in an emulation system (Swoboda: Fig.2 & associated disclosure), comprising receiving a first sample of state data (Swoboda: Fig.9 & and associated disclosure); selecting a first data of interest from the first sample of state data (Swoboda: Fig.9 state data having at least Data, Address, PC"), wherein the data of interest is a subset of bits of first sample of state data and includes at least first and second portions separated from each other by at least one bit that is not part of the data of interest (Swoboda: Fig.19 & [0121]).

Further Swoboda teaches storing the first data for transmission such that first and second portions of the first *data of interest* ***are*** *no longer separated* by at least a bit as selecting the first data of interest from the packet (Swoboda: Fig.19 & [0121], See Data Byte 1 and Data Byte 2) and then aligning them for transmission (Swoboda: [0122]-[0128], [0130] & Fig.2, 8, 21, 22 and 23, 23 A-B).

Swoboda teaches receiving second sample state data (Swoboda: [0094] at least, [0121] & Fig.19). Swoboda also teaches selecting a second data of interest from the second sample of state data, wherein the second data of interest is a second subset of bits of the second sample of state data and wherein bit locations of the first data

of interest and the second data of interest are different as constant stream of trace information (Swoboda: Fig.1), where a sample format (Fig.19 and 9) may vary and bytes are selected according to rationale presented in (Swoboda: [0121]) and transmitted to stream combiner (Swoboda: Fig.22).

Although Swoboda is concerned with storage of trace information, through compression (Swoboda: [0117]-[0118]) it does not explicitly teach determining residual storage of trace buffer and selecting the next buffer if the first buffer is full.

Litt teaches determining if residual storage space in a first buffer exists as smart buffers, which are aware of the buffer state (full or available) of each location in the smart buffer (Litt: Col.10 Lines 12-46). Litt also teaches receiving a first sample of state data (Litt: Col.8 Lines 33-48), sorting the first sample (Litt: Col.7 Lines 20-67), and storing the sorted first sample of state data in the smart buffer (Litt: Fig.2).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Litt to Swoboda as Litt & Swoboda are primary concerned with offloading the trace information. The motivation to combine would be that Litt provides arbitration logic to unload multiple trace buffer (Litt: Fig.2 & associated text) lacking in Swoboda to ease the unloading pressure making the system run faster with appropriate prioritization, especially when trace offloading rates are different from trace generation rate (Swoboda: Fig.22, [0128]-[0129]).

Litt in Swoboda do not explicitly teach switching to the second buffer if the first buffer is full for storing the trace information.

Tausheck teaches checking if residual space in the first buffer exists, storing the data in it and if the first buffer is full then storing the data in second buffer (Tausheck: Col.2 Lines 38-45).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Tausheck to Litt & Swoboda as Litt & Swoboda are primary concerned with offloading the trace information, however do not disclose handling of multiple offload buffers. The motivation to combine would be that Litt and Swoboda disclose buffer which are FIFO buffer (Litt: Col.10 Lines 13-37; Swoboda: [0128]), however buffer switching is not disclosed by either to ease buffer pressure and overflow condition, which is taught by Tausheck as handing multiple DMA buffers is an analogous situation where switching happens between the full buffers (Tausheck: Abstract).

Regarding Claim 2

Litt teaches the step of determining whether the first buffer is full and storing the *data of interest* as first sample in the first buffer (Litt: Col.10 Lines 17-46).

Regarding Claim 8 (Updated 2/12/09)

Swoboda teaches storing the second data of interest from the second sample of state data (Swoboda: Fig,1 and [0094], Also see [0109] and Fig,8-9).

Regarding Claim 9

Litt & Tausheck teach smart buffers that decide based on the residual space left in the buffer whether to store the data (Litt: Col.10 Lines 47-60; Tausheck: Fig.3). Swoboda also teaches storing partial information in the buffer (Swoboda: Fig.19).

Applicant has qualified the data as “state data” and subset of that as “data of interest”. These qualifications do not alter the methodology and is intended use of the method.

Regarding Claim 10

Swoboda teaches receiving comprises receiving the first sample of state data from reconfigurable emulation resource (Swoboda: Fig.2-4 [0007][0066]).

Regarding Claim 16

Litt teaches step of storing sample information associates with each sample as importance control bit (Litt: Col.9 Line 45 – Col.10 Line 12). Applicant has qualified the data as “state data” and subset of that as “data of interest”. These qualifications do not alter the methodology and is intended use of the method.

Regarding Claim 17

Litt teaches storing the importance/control of the sample based on the position/length of the sample header. This counter associated stores the bit position of the ticks (segments of the sample – See Col.6 Lines 49-60) of the sample (Litt: Col.14 Lines 5-23; Col.10 Lines 47-60). Applicant has qualified the data as “state data” and subset of that as “data of interest”. These qualifications do not alter the methodology and is intended use of the method.

Regarding Claim 18

Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted (Swoboda: Fig.22; [0128]). Applicant has qualified the

data as "state data" and subset of that as "data of interest". These qualifications do not alter the methodology and is intended use of the method.

Regarding Claim 19 (Updated 2/12/09)

Claim 19 repeats the limitations of claims 1 & 16, where the subsequent packets are stored in the memory and is rejected for the same reasons as parent claims. Also see Swoboda Fig.22 and 22A. Applicant has qualified the data as "state data" and subset of that as "data of interest". These qualifications do not alter the methodology and is intended use of the method. *Swoboda teaches selecting data of interest from the second sample of state data as repetition of the same methodology as for first sample (Swoboda: Fig.19 & [0121]), wherein the data of interest is a subset of bits of the second sample of state data and includes at least first and second portions separated from each other by at least one bit that is not part of the data of interest (Swoboda: Fig.19 & [0121], See Data Byte 2 and Data Byte 5).* Plurality of state data and data of interest would be obvious in view of Fig.2 of Swoboda.

Regarding Claim 20 (Updated 2/12/09)

Litt teaches an apparatus having a first select logic device configured to receive samples of state data, to sort samples of state data, and to select data of interest from each of the samples of state data (Litt: Fig.2, Elements 210 & 215, Col.6 Lines 3-34).

Swoboda teaches wherein selected bit locations of the data of interest from at least two samples are different as it is obvious that not every sample state data layout would look identical to the exemplary sequence presented in Swoboda Fig.19.

A different sequence of bytes, other than the one listed in Fig.19, would result in different bytes selected based on rationale presented in [0121]. Therefore Swoboda teaches this limitation.

Litt teaches first and second buffers coupled to the first select logic device and configured to receive the selected data of interest (Litt: Fig.2 Elements 225a 225b); a second select logic device coupled to the first and second buffers and configured to select the first and second buffers in an alternating manner to drain the selected buffer (Litt: Fig.2 Elements 250); and an output storage device coupled to the second select logic device and configured to receive data drained from the selected buffer (Litt: Fig.1 Element 50).

Litt does not teach select data of interest being filled in an alternating manner in each buffer.

Tausheck teaches that trace data is filled in the alternating manner in the trace buffers and then emptied in the alternating manner (Tausheck: Col.5 Lines 62-Col.6 Lines 67 at least).

Regarding Claim 21

Litt teaches first select logic comprises a multiplexer (Litt: Fig.2 Elements 245a & 245b).

Regarding Claim 22

Litt teaches second select logic (as arbitration logic) comprises a multiplexer (Litt: Fig.2 Elements 250; Col.11 Line 56-Col.12 Line 43) where the selection between the buffers to offload the data of interest from them.

Regarding Claim 23

Litt & Tausheck teach first select logic device (Litt: 245a & b) is configured to send data if interest to second buffer responsive to first buffer becoming full (Tausheck: Col.5 Lines 62-Col.6 Lines 67 at least).

Regarding Claim 24

Litt teaches the first select logic device comprises a data of interest sorter (Litt: Fig.2 Packet Prediction and parsing logic with the Prioritization of packets; Col.10 Lines 47-Col.11 Line 6).

Regarding Claim 25

Claim 25 discloses similar limitations as claim 16 and is rejected for the same reasons as claim 16. Litt teaches step of storing sample information associates with each sample as importance control bit (Litt: Col.9 Line 45 – Col.10 Line 12).

Regarding Claim 26

Claim 26 discloses similar limitations as claim 17 and is rejected for the same reasons as claim 17. Litt teaches storing the importance/control of the sample based on the position/length of the sample header. This counter associated stores the bit position of the ticks (segments of the sample – See Col.6 Lines 49-60) of the sample (Litt: Col.14 Lines 5-23; Col.10 Lines 47-60).

Regarding Claim 27

Claim 27 discloses similar limitations as claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 28

Litt teaches output storage device is configured to store information associated with each of the samples of state data as header to each sample that contains sample relevant data (Litt: Col.6 Line 61- Col.7 Line 19).

Regarding Claim 29 (Updated 2/12/09)

Litt teaches determining a trace data fill rate of each of a plurality of trace data chains as various trace streams with various rates in the bandwidth manager section (Litt: Col.4 Lines 21-25, 55-65); determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates as decision to offload data by the arbitration manager based on the pressure on the trace buffer once it gets full due to higher fill rate (Litt: Col.12 Lines 8-31).

Litt does not teach a pin manager explicitly that would perform the steps of offloading the data.

Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted (Swoboda: Fig.22; [0128]).

Swoboda teaches one of the plurality of pins is shared by at least two trace data chains as plurality of pins in the trace output ([0017], [0051], [0052], [0058], [0073], [0092], [0094] at least) where there are plurality of trace data chains (See Fig,2, Trace Inputs and Identify information forming trace data chains collected by Trace Collection 21).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Swoboda to Litt to enhances the Litt's teaching by adding a Pin Manager/macro function to arbitration logic and output section of Litt's teaching. To clarify further, The motivation to combine would have been that Swoboda and Litt are concerned with trace data capture where Swoboda and Litt output the trace data to a debugger (Litt: Fig.2; Swoboda: Fig.2, 22, 23, 23A-B) where the pin management is obvious for such data offloading. Swoboda explicitly discloses the pin manager, where the pins for trace & debug can be dynamically allocated reducing the limited pin count pressure in offloading trace information (Swoboda: Fig.22; [0128]).

Regarding Claim 30 (Updated 2/12/09)

Claim 30 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29. The bandwidth allotment is determined by the arbitration logic and directions from source clock (Litt: Col.12 Lines 57-Col.13 Line 27). Litt does not explicitly teach the pin schedule selection, which is taught by Swoboda (Swoboda: Col.10 Lines 3-4).

Swoboda teaches one of the plurality of pins is shared by at least two trace data chains as plurality of pins in the trace output ([0017], [0051], [0052], [0058], [0073], [0092], [0094] at least) where there are plurality of trace data chains (See Fig,2, Trace Inputs and Identify information forming trace data chains collected by Trace Collection 21).

Motivation to combine Litt and Swoboda is the same as claim 29 above.

Regarding Claim 31 (Updated 2/12/09)

Claim 31 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30. Litt teaches the limitation where the trace chain data fill rates are determined and matched with the data output rate from the arbitration logic. Arbitration logic multiplexer selects the input (pins) from smart buffer based on the fill rate and distress (due to higher fill rate in a smart buffer) (Litt: Col.11 Lines 56-Col.13 Line 37.

Swoboda teaches one of the plurality of pins is shared by at least two trace data chains as plurality of pins in the trace output ([0017], [0051], [0052], [0058], [0073], [0092], [0094] at least) where there are plurality of trace data chains (See Fig,2, Trace Inputs and Identify information forming trace data chains collected by Trace Collection 21).

Motivation to combine Litt and Swoboda is the same as claim 29 above.

Regarding Claim 32 (Updated 2/12/09)

Swoboda teaches a second packet handling similar to the first packet handling (Swoboda: Fig.19, 22A, Fig.23, 23A-B). Litt teaches storing in either of first and second buffers (Litt: Fig.2 225a and 225b). Swoboda also teaches, data of interest not separated by one bit (Swoboda: Fig.19 Data bytes 1 & 2). Plurality of state data and data of interest would be obvious in view of Fig.2 of Swoboda.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AKASH SAXENA whose telephone number is (571)272-8351. The examiner can normally be reached on 8:00- 6:00 PM Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128

/Akash Saxena/
Examiner, Art Unit 2128